A PIN DIODE SWITCH THAT OPERATES AT 100 WATTS CW AT C-BAND

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ABSTRACT

Measured data on a packaged 6 port matrix switch yields an insertion loss of 1.2 dB maximum and isolation of 60 dB minimum from 4.2 to 5.2 GHz. The phase balanced switch handles 100 watts CW in the frequency band at temperatures of -30 to +95C.

INTRODUCTION

Microwave silicon PIN diode switches are becoming common place in todays defense market because of the characteristics of small size, light weight, and power handling capabilities. Other switches can give smaller size or higher power handling, but not both. One alternative is the MMIC GaAs FET switch. It beats the PIN diode switch in both size and weight. Yet, it has poor power handling ability. On the other end of the power spectrum are the mechanical or ferrite switches. They typically handle more power than PIN switches, but their size, reliability and weight limit their usefulness. With the development of better silicon processing over the years, PIN diodes are providing the means for microwave switches that handle microwatts to several kilowatts[1-2] CW!

With computer optimization and microwave measurement, a packaged 6 port PIN diode matrix switch was developed. The switch is shown in figure 1. A conventional shunt diode design was chosen to provide a good thermal path for enhanced reliability. Each arm of the common junction switch contains 2 diodes that are separated by a high impedance line. Each line provides an impedance such that its VSWR cancels with each of the other lines creating a -20dB return loss, 1.2dB insertion loss, 60 dB isolation, and 100 watt CW power handling from 4.2 to 5.2 GHz.

The design approach will be described with practical techniques that made this design possible. Also, measured S-parameters and insertion loss vs. input power over temperature are provided.

CIRCUIT DESIGN

The complete design of the switch had four segments. Diode power handling mechanisms were examined so that a suitable PIN diode could be chosen. The PIN diodes had to be characterized and modeled for insertion into Touchstone. All circuit losses were computed to determine the amount of dissipation in each part of the switch. Also, a thermal model was needed so that a suitable package could be developed.

Diode power handling: There are 2 diode failure mechanisms related to power handling. One for each bias state. In the forward bias state the diode represents a resistance (R_S) that in this case is 0.7 ohm. This resistance causes (I^2R) heating in the diode junction due to both dc current (50mA bias) and RF current. According to White[3], temperatures over 300C cause metal-silicon alloys to form across the intrinsic region of the diode. Low diode junction temperature is needed because PIN diode life expectancy is inversely porportional to the junction temperature of the diode. A maximum junction temperature of 105C was chosen for this design to ensure a reliability of 10^7 hours. In the diode reverse bias state, the failure is due to the peak voltage swing of the RF signal on top of the reverse bias. For this design the required RF power level was 100 watts CW.

$P_{max} = [V^2 / (8*Z_0)]$ for a single shunt diode (1)

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From equation (1) the RF peak voltage[4] is 200 volts. A diode with a reverse breakdown of 400 volts was chosen for this design. It was biased at -95 volts to minimize the 2nd harmonic.

The power capabilities of other components: Other considerations were the substrate material and connector type. A substrate material of 25 mil thick Alumina was chosen because it can handle 5.26 kilowatts compared with 378 watts for Teflon substrates[5]. SMA connector temperatures rise to 70C with an incident power of 100 watts CW. Several SMA connectors were tested with no failures.

Pin diode model: Two diode models were developed. One model was for the resistive state (positive bias) and the other for the capacitive state (reverse bias). The resistance (R_S) was determined from the isolation produced from one diode. The diode was mounted in a 50 ohm microstrip line and the resistance determined from[6]:

$$\text{Isolation} = -10*\log_{10}(1+Z_o/R_S+Z_o^2/[4*R_S^2]) \quad (2)$$

An insertion loss of -30.7dB was measured at 45MHz with a forward diode bias of 100mA. From equation (2) R_s is 0.7 ohms. The wire bond inductances were calculated using Terman's equation[7]:

$$L = 0.00508*l*(2.303*\log_{10}(4*l/d)-1)*10^3 \text{ nH} \quad (3)$$

A wire bond with dimensions of 0.001in x 0.033in yields an inductance of 0.65 nH. To determine the capacitance C_J, a diode was mounted shunt to ground between 50 ohm transmission lines on 25 mil alumina. Each 50 ohm line was connected to the diode through 1 mil x 33 mil bond wires. To minimize parasitics, the diode was mounted on a 15 mil pedestal within a 75 mil hole. The top of the diode was coplanar with the surface of the alumina. Using an HP-8510, S-parameters were measured. C_J was fitted to the measured data using Touchstone, and was found to be 0.5 pF.

Circuit optimization: A Touchstone circuit file, shown in figure 2, was developed with transmission lines, wire bonds, and diodes for the symmetric matrix switch. Bias decoupling, capacitors, connectors, etc. were not included in the optimization to allow for a fast convergence. The effects of these components are added as separate losses. Three optimization variables were used. The length of the transmission line between diode and the switch junction as well as the length and width of the transmission line between the two diodes of each arm were allowed to vary. The conditions of convergence are mag[s11]=0 and mag[s22]=0. This optimized circuit file provided the dimensions for the transmission line circuit layout.

Circuit losses: The theoretical loss of the matrix switch is determined by considering the loss of every component in the switch. Each individual loss must be minimized to reduce the amount of dissipated power.

Connector Loss	**-0.1 dB**
Line Loss	**-0.3 dB**
Capacitor Loss	**-0.2 dB**
Mismatch Los	**-0.1 dB**

Diode Loss (forward bias)

50 ohm / 0.7 ohm = 71.4 denormalize

71.4 / 4 = 18 4 parallel resistors

$I_{loss} = 20*\log(2 / [2+1/18])$

-0.25 dB

Diode Loss (reverse bias)

5K ohms / 50 = 100 denormalize

$I_{loss} = 4*20*\log(2 / [2+1/100])$

-0.2 dB

$$\text{Loss}_{total} = \textbf{-1.1 dB}$$

The measured insertion loss was -1.2 dB. This is shown in Figure 4. For an incident power of 100 watts CW, that equates to a dissipated power of 24 watts.

Thermal model and package design: To do a thermal analysis, dissipated power for each element was determined. For an input power of 100 watts CW and starting from the input to the switch and walking through each component, the dissipation in the diode was found to be 1 watt. The system specified a maximum base plate temperature of 90C. To meet our design constrant of 120C diode junction temperature, each diode was mounted on a gold plated molybdenum tab 15 mils thick. Because of the 120C temperature, the alumina substrate was placed on a 50 mil thick molybdenum carrier. This is because of the high temperature coefficient of expansion of Alumina. The complete thermal path for a diode include the moly tab, moly carrier, and aluminum package. A thermal analysis was performed using the

computer program[8] listed in Arkin's paper. The diode temperature was predicted to be less than 105C.

SWITCH PERFORMANCE

The first iteration of the switch did not meet the 50 dB isolation spec. This was due to the bias decoupling circuits. The bias circuit was built and improved using larger decoupling capacitors. The measured input match and isolation are shown in Figure 3. The input match shows a double resonance which gives the switch larger bandwidth. The insertion loss is shown in Figure 4. The rejection in the skirts of this bandpass response does not decay quickly. If more diodes were used, more rejection would result.

There was a concern that over temperature and power the switch loss would vary significantly. The switch was built and tested at -30C, 25C, and 95C from 15 watts to 100 watts CW. This is shown in Figure 5. From -30C to +95C the insertion loss only varies 0.1dB. From 15 to 100 watts CW the insertion loss varies by 0.2dB.

CONCLUSION

A small, low loss, high power switch matrix has been developed using PIN diodes. A composite switch design was accomplished using many design segments. After the appropriate high power PIN diodes were chosen, measured, and modeled, a theoretical shunt diode design was optimized neglecting losses. Then the individual loss of each component was minimized and combined to come up with the total switch loss. The amount of power dissipated in each component was analyzed with a thermal analysis program. This lead directly to the package design.

Susequently, 110 switches were fabricated on a contractual program. To date, only one switch has failed in a fielded system.

Other implementations of this approach have been investigated including a series diode design on Berillium Oxide (BeO). This appeared feasible for even higher power levels. It was not fielded because of the toxic nature of BeO dust.

REFERENCES

[1] R. Tenenholtz, "A 2000 watt CW MIC 20-500 Mhz SPDT PIN Diode Switch Module," IEEE Int'l Microwave Symposium, pp.252-254,1981.

[2] D. W. Kintigh and W. K. Niblack, "High-Power 2-9 Ghz Solid State Switch," IEEE Int'l Microwave Symposium, pp. 54-56, 1982.

[3] Joseph F. White, Semiconductor Control, Artech House, 1977, p.80.

[4] Robert V. Garver, Microwave Diode Control Devices, Artech House, 1976, p. 107.

[5] I. J. Bahl and K. C. Gupta, "Average power-handling capability of microstriplines", Microwaves, Optics and Acoustics, pp.1-4,Jan 1979.

[6] Paul Chorney, "Multi-Octave, Multi-Throw, PIN-Diode Switches,"The Microwave Journal, pp. 39-48, September 1974.

[7] Frederick Terman, Radio Engineers' Handbook, McGraw-Hill, 1943, p. 49.

[8] O Arkin, "Practical Computer Program for Improved Hybrid Thermal Analysis,"Hybrid Circuit Technology, pp. 37-42, Nov 1986.

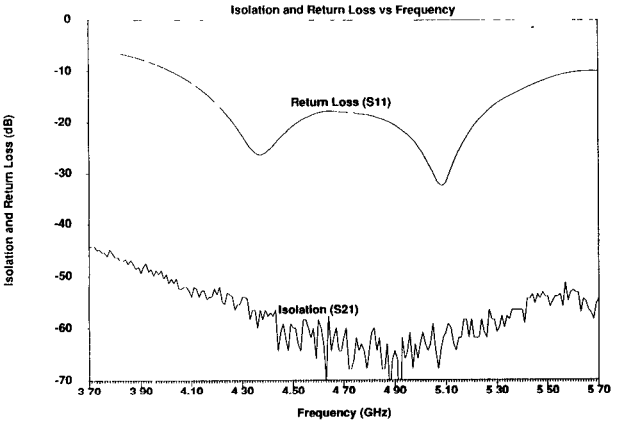
Figure 2. Touchstone Circuit File.

```
VAR
LINE1 # 25 200 300
LINE2 # 25 114 300
W2 # 10 12.5 40
INLINE # 25 25 200
! Alumina Substrate
CKT
MSUB ER=9.9 H=25 T=.25 RHO=1 RGH=0
TAND TAND=0.001
! Diode Model 'on'
IND 1 2 L=.65
RES 2 0 R=.7
IND 2 3 L=.65
DEF2P 1 3 DON
! Diode Model 'off'
IND 1 2 L=.65
CAP 2 0 C=.5
IND 2 3 L=.65
DEF2P 1 3 DOFF
! Diode Model 'off'
MLIN 1 3 W=23.5 L^LINE1
DON 3 4
MLIN 4 5 W^W2 L^LINE2
DON 5 6
MLIN 6 7 W=23.5 L=100
DEF2P 1 7 OFF
! Arm Model 'on'
MLIN 1 3 W=23.5 L^LINE1
DOFF 3 4
MLIN 4 5 W^W2 L^LINE2
DOFF 5 6
MLIN 6 7 W=23.5 L=100
DEF2P 1 7 ON
! Complete Switch
ON 1 4
OFF 1 5
MLIN 4 25 W=2.5 L=260
MLIN 5 25 W=2.5 L=260
MLIN 1 2 W=23.5 L^INLINE
OFF 2 21
OFF 2 22
OFF 2 23
ON 2 3
MLIN 21 25 W=2.5 L=260
MLIN 22 25 W=2.5 L=260
MLIN 23 25 W=2.5 L=260
MLIN 3 25 W=2.5 L=260
CAP 25 0 C=248
RES 21 0 R=50
RES 22 0 R=50
RES 23 0 R=50
DEF3P 4 3 5 SWITCH

FREQ
SWEEP 3.7 5.7 .1

OUT
LINE DB[S21] GR1
SWITCH DB[S21] GR1 > -.5
SWITCH DB[S11] GR2
SWITCH DB[S22] GR2
SWITCH DB[S31] GR2
! Optimize for perfect match
OPT
SWITCH MAG[S11]=0
SWITCH MAG[S22]=0
```

Figure 3. Measured Isolation and Return Loss



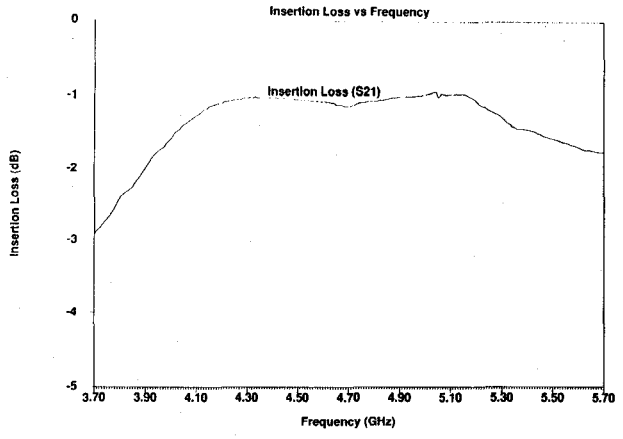


Figure 4. Measured Insertion Loss

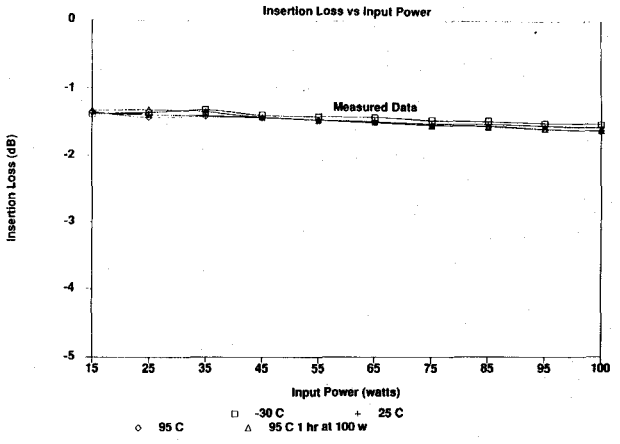


Figure 5. Measured Insertion Loss vs. Input power From -30C to +95C.

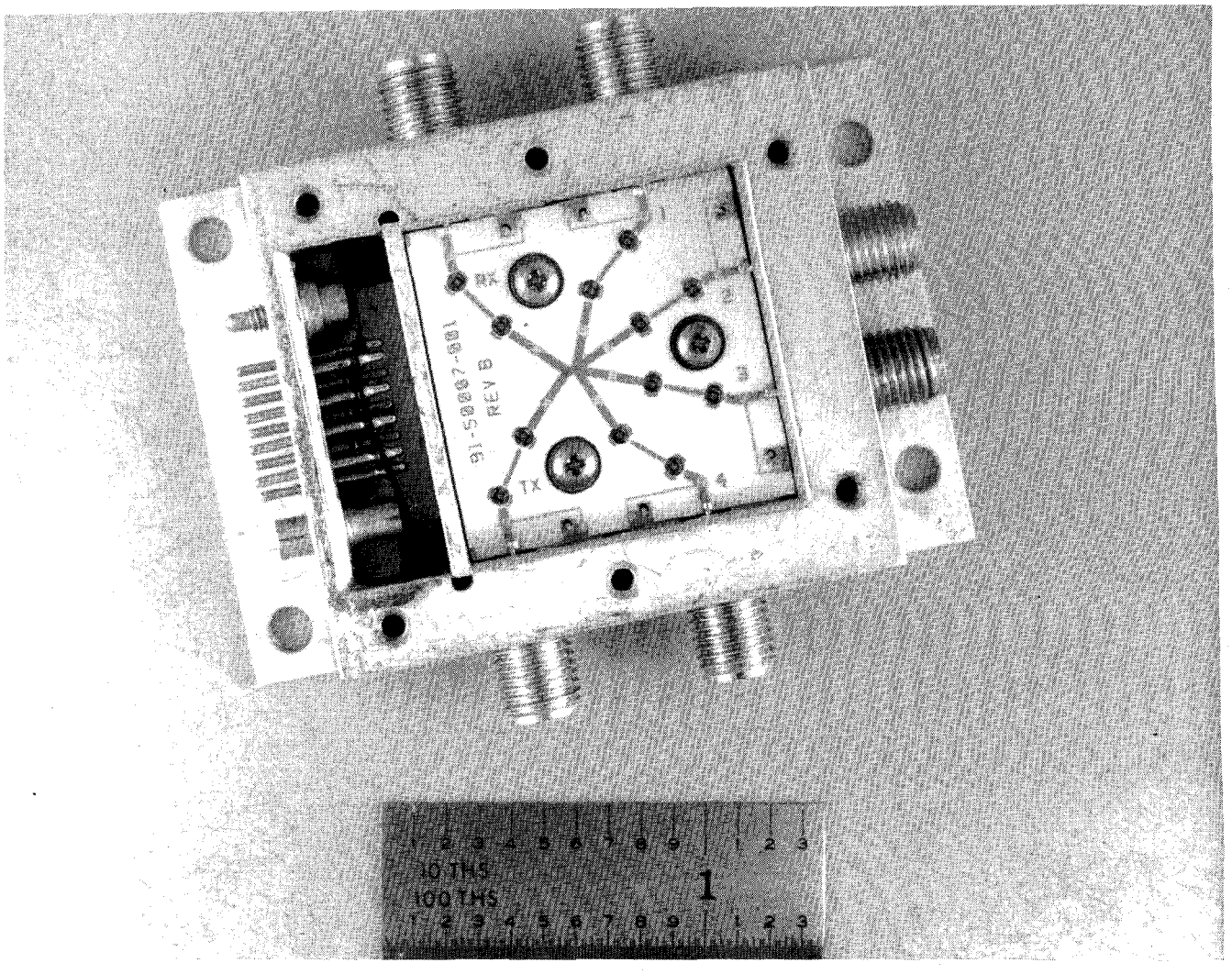


Figure 1. Six Port Matrix Switch.